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ANALYSIS, DESIGN & SIMULATION OF ANALOG TO DIGITAL CONVERTER

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ABSTRACT

In this work, I successfully designed the 4-bit SAR ADC and 12 bit cyclic ADC and successfully measured the parameters of ADC by non-metrics curve and quantization curve. My motive was to design a 12-bit SAR ADC but because of clock skew, and signal integration in different sub-blocks, I could have designed the 4-bit SAR ADC.

The Sub-blocks of SAR ADC and Cyclic ADC are 80 % same that's why I completed 12 bit Cyclic ADC, in which there is less problem of clock skew, and signal integration. All building blocks of SAR and Cyclic ADC were successfully simulated.

KEYWORDS: *Simulation of Analog, Digital Converter*

INTRODUCTION

Advantages of "digital circuits" that helps a solid motivation to build "the world digital", there are features of our "physical environment impede globalization". "Firstly the naturally occurring signals are analog and secondly human beings perceive and retain information in analog form." When digitized signs are disturbed by the intermediate such that "they become differentiable with noise, it is often important to handle them as analog signals".

The analog to digital interface changes a "continuous-amplitude, continuous-time input to a discrete-amplitude, discrete-time signal". A pre filter called an anti-aliasing filter is importantly to avoid the aliasing of higher frequency signals back into the base band of the ADC. Often the anti-aliasing filter is implemented by the band limiting characteristics of the ADC itself. The ant aliasing filter is followed by a sample and hold circuit that helps the input analog signals to the ADC constant when the time this signal is converted to an corresponding digital output code. This period of time is called the conversion time of the ADC. The conversion is proficiently by a quantization step. The nature of a quantizer is to segment the reference into sub range. The quantization step catches the sub range that relates to the sampled analog input. Knowing this sub range permits "the digital processor to encode the equivalent digital bits. Thus, within the conversion time, a sampled analog input signal is converted to a corresponding digital output code". [7]

Why ADC

For a long time, ADCs have been used widely in digital test equipment. In recent times, the applications for "ADCs have extended widely as many electronic systems that helps to be whole analog have been executed using digital electronics". "Examples of such applications include digital telephone transmission, cordless phones, transportation, and medical imaging." Furthermore, ADCs have start their way into systems that would generally be considered as being totally digital as these digital

systems are pressed to higher levels of performance. Data storage is the example of such a system. As storage thickness in disk drive systems is improved, the signals handled by the read circuitry have become higher analog in character.

BACKGROUND

In mixed signal design, "data conversion provides the link between the analog world and digital system and is performed by means of sampling circuits, analog to digital converter and digital to analog converter". "With the increasing use of digital computing and signal processing in application such as medical imaging, instrumentation, consumer electronics and communication, the field of data conversion system has rapidly expanded over the past twenty years".

THE ADC ARCHITECTURE AND IMPLEMENTATION

The Cyclic and SAR ADC prototype was designed in mentor tool using 0.35µm CMOS process. In previous chapters the basic data conversion principles were discussed. Understanding these concepts provides the necessary knowledge for proper ADC design. The rest of this chapter focuses on describing the circuit design of the SAR ADC prototype. The design choices made for each circuit block are discussed and their respective performance specifications are presented through analytical calculations and simulations.

Figure 1 illustrates the block diagram of the ADC prototype. It consists of an S/H circuit, a DAC, a comparator, and digital logic. The latter implements the successive approximation algorithm and generates the necessary control signals to synchronize the operation of all the ADC circuit blocks.

Figure 1: SAR ADC Architecture

Architecture of the ADC

The ADC architecture that we have implemented is based on cyclic ADC architecture [3]. The ADC architecture is shown in Figure 2.

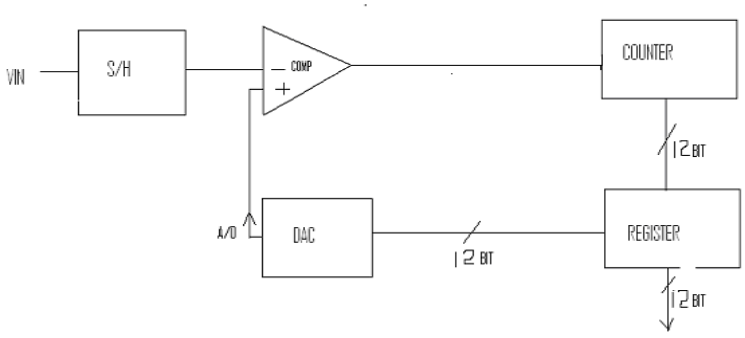

Figure 2: Cyclic ADC Architecture.

Schematic of 8 Bit ADC

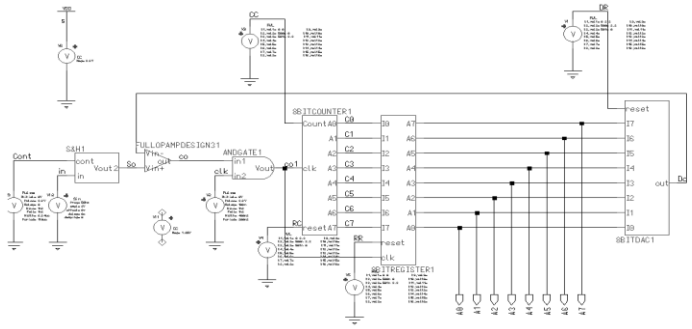

Figure 3: Schematic of Cyclic ADC.

EXPERIMENTAL RESULTS

Results of simulations are well presented in this paper by using Mentor Graphics tool with specifications in below Table.

Table 1: Specifications of 12 Bit ADC

S. No	Specification	Measured
Sampling Frequency	1.5 MHz	1MHz (required)
Conversion Time	410ns	300ns (required)
VLSB	12 mV	12 mV
Resolution	4096	4096
INL	.5 LSB	1 LSB
DNL	.5LSB	2 LSB
Offset error	0 LSB	0 LSB
Gain Error	.5 LSB	2 LSB

Testing of 8-Bit ADC

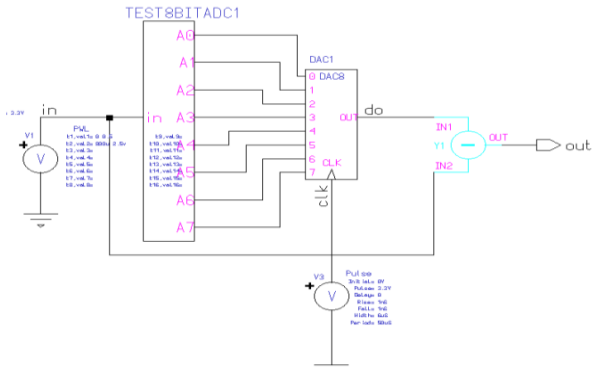

Figure 4: Testing of 8 bit ADC.

Straight Line Transfer Functions

An endpoint straight line fit compares the converter's actual transfer function with an ideal transfer function determined by the converter's zero and full scale inputs. The endpoint straight line transfer function is the straight line between the midpoints of the converter's zero scale and full scale values. The best fit straight line fit compares the actual converter transfer curve with an ideal transfer function found by minimizing a cost function, typically RMS error. Therefore, the best fit straight line transfer function represents straight line which "best" approximates the converter's transfer function. An endpoint straight line transfer function for a non-ideal ADC is shown in Figure 4.

Integral Nonlinearity

A converter's integral nonlinearity (INL), also called integral linearity error, is defined as the difference between the converter's transfer function and the converter's straight line transfer function. INL is the single most important measure of a converter's linearity. Many data converter data sheets only report the maximum value of the INL curve. Figure 4 shows The maximum INL of a non-ideal 12 bit ADC. Figure 5 shows the maximum INL of an ideal three bit DAC.

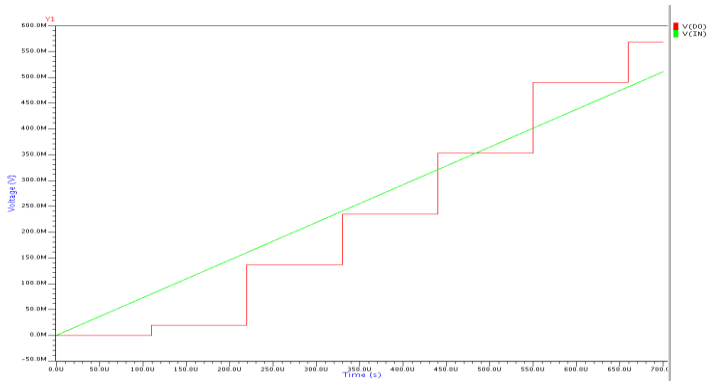

Figure 5: INL & DNL Curve.

Differential Nonlinearity

A converter's differential nonlinearity (DNL), also called differential linearity error, is defined as the difference between the converter's ideal code widths and the converter's actual code widths.

Adjacent digital codes should be associated with analog values which differ by an ideal code width, i.e. full scale range divided by the number of codes. The difference between the converter's actual code widths and the ideal code widths is DNL. Many data converter data sheets only report the maximum value of the DNL curve. Figure 4 shows the maximum DNL for a non-ideal 12 bit ADC. Figure 5 shows the maximum DNL for an ideal 12 bit DAC.

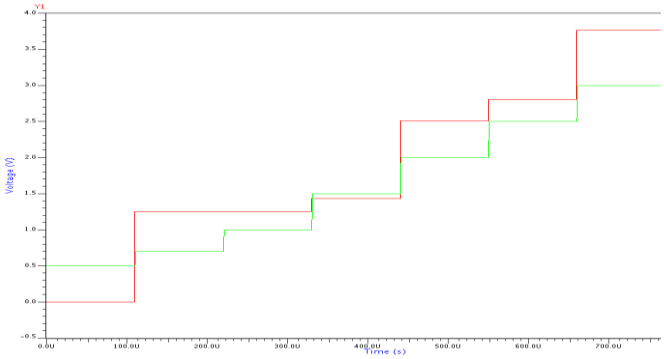

Figure 6: Nonlinearity Metrics.

ADC Zero Offset Error

ADC zero offset error, zero scale error or zero code error, is the difference between the ADC's ideal zero scale, i.e. ground for unipolar ADCs and negative full scale input for bipolar ADCs, and the ADC's actual zero scale input. Many ADCs have zero offset error adjustment so that zero offset error can be made zero. ADC zero offset errors are usually caused by nonzero input-offset voltage or input offset currents in the ADC's amplifiers or comparators.

Gain Error

The gain error, illustrated in Figure 5, is the difference in slopes between the actual transfer characteristic of an ADC and that of an ideal one.

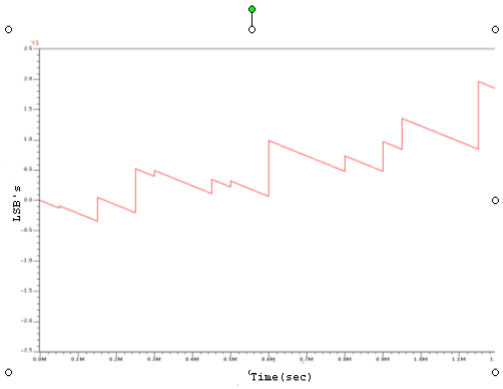

Figure 7: Quantization Curve.

CONCLUSIONS

In this paper, designed 8 bit cyclic ADC. And also find the parameters of ADC by non-metrics curve and quantization curve. All building blocks of SAR and Cyclic ADC were successfully simulated.

A to D converter is realized in a 0.35 □m technology with a double ended 3.3V source voltage with a lively area of 1.26 mm2. The extreme resolution of our A to D Converter is 8 bits with a determined assessed power dissipation of 6.35 mW.

My motive was to design an 8-bit SAR ADC but because of clock skew, and signal integration in different sub-blocks, I could have designed the 4-bit SAR ADC

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